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| EXAMINER | |
|---|---|
| DANG, KHANH | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2111 | |

DATE MAILED: 05/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/630,460 | EMMOT ET AL. | |
| | Examiner | Art Unit | |
| | Khanh Dang | 2111 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-24* is/are rejected.

7)☒ Claim(s) *3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

Claims 11-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 11, the phrase, "logic for controlling the selective communication of information received from by the first logic interface" (emphasis added) is unclear.

In claim 12, the word "through: is a typing error.

In claim 20, the language "the number of total conductive pins of the integrated circuit component is fewer than the number of conductive pins of a corresponding conventional integrated circuit component" renders the claim indefinite, since it is unclear what number may be the "number of conductive pins of a conventional integrated circuit component."

Claims 1-10 are directed to an apparatus. However, the essential structural cooperative relationships between elements in the claims such as "logic" (line 2), "logic" (line 4), "logic for controlling," "first portion of system bus," "second portion of system bus," "integrated circuit component," and "second integrated circuit component" have been omitted, such omission amounting to a gap between the necessary structural connections. MPEP 2172.01.

Claims 10-19 are directed to an apparatus. However, the essential structural cooperative relationships between elements in the claims such as "first logic", "second logic", "logic for controlling," "portion of system bus," "plurality of companion integrated

circuit components" "integrated circuit component," and "remote component" have been omitted, such omission amounting to a gap between the necessary structural connections. MPEP 2172.01.

Claims 20-24 are directed to an apparatus. However, the essential structural cooperative relationships between elements in the claims such as "first set of conductive pins," "second of conductive pins," "additional conductive pins," "portion of a system bus," "integrated circuit component," and "companion integrated circuit component" have been omitted, such omission amounting to a gap between the necessary structural connections. MPEP 2172.01.

MPEP 2172.01 requires that relationships between elements recited in claims must be specified. Specifically, MPEP requires interrelation and structural relationships between essential elements in the claims. It is the Examiner's position that, the claimed elements, as defined in the originally filed specification and identified above, are essential elements to the claimed invention. Since they are essential elements as defined by the originally filed specification, their structural cooperative relationships must be provided in the claims. Further, it is also the Examiner's position that the claimed elements as identified above, function simultaneously, are directly functionally related, directly intercooperate, and/or serve independent purposes, as evidenced from the originally filed specification. If Applicant does not agree with the Examiner that the claimed elements as defined by the specification and identified above, are not essential elements to the claimed invention, Applicant is required to state on the record that this is the case.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 4-13, and 15-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Estakhri et al. (Estakhri, 6,172,906).

As broadly drafted, these claims do not define any structure that differs from Estakhri.

With regard to claim 1, Estakhri discloses an integrated circuit component (shown generally at Figs. 1 and 6a) comprising: logic (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 comprises "logic"; see at least column 2, lines 28-37; column 6, lines 57-65) capable of being configured to interface with a first portion of a system bus (28/680; column 1, line 31 to column 2, line 3; column 7, line 1-9); and logic (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673

comprises the so-called "logic"; see at least column 2, lines 28-37; column 6, lines 57-65) capable of being configured to interface with a companion integrated circuit (18/670 or 20/672; column 1, line 31 to column 2, line 3; column 6, lines 57-65) and to receive information that is communicated from the companion integrated circuit, which information was communicated to the companion integrated circuit via a second portion of the system bus (38/684; column 1, line 31 to column 3, line 2; column 7, lines 1-9).

With regard to claim 2, Estakhri further discloses a link layer control logic in both the logic capable of being configured to interface with the first portion of the system bus and the logic capable of being configured to interface with the companion integrated circuit (it is clear that the controller (12/510; column 1, line 31 to column 2, line 3; column 6, lines 10-29) linking both logics to provide unified bus logic configured to consolidate information received from both logics interfaced with the first portion of the system bus (28/260; column 1, line 31 to column 2, line 3; column 7, line 1-9) and the companion integrated circuit 18/670 or 20/672), the link layer control logic (12/510; column 1, line 31 to column 2, line 3; column 6, lines 10-29) being configured to exchange link layer control information, such that both the logic capable of being configured to interface with the first portion of the system bus and the logic capable of being configured to interface with the companion integrated circuit (both logics interfaced with the first portion of the system bus (28/680; column 1, line 31 to column 2, line 3; column 7, line 1-9) and the companion integrated circuit 18/670 or 20/672; column 1, line 31 to column 2, line 3; column 6, lines 57-65) possess complete link layer control information for the data being communicated over the system bus (it is clear that

the controller (12/510; column 1, line 31 to column 2, line 3; column 6, lines 10-29) provides unified bus logic configured to consolidate information received from both logics interfaced with the first portion of the system bus (28/680; column 1, line 31 to column 2, line 3; column 7, line 1-9) and the companion integrated circuit 18/670 or 20/672; column 1, line 31 to column 2, line 3; column 6, lines 57-65).

With regard to claim 4, it is clear that the controller (12/510) provides unified bus logic configured to consolidate information received from both logics interfaced with the first portion of the system bus 28/260 and the companion integrated circuit 18/670 or 20/672).

With regard to claim 5, it is clear that the controller (12/510) or the so-called "functional logic" performs at least one logic operation for the integrated circuit component.

With regard to claim 6, it is clear that the system bus comprising two split buses 28/260 and 38/684 is a point-to-point serial communication bus.

With regard to claim 7, it is clear that the memory controller (12/510) or the so-called "functional logic" performs the logic operation of a memory controller.

With regard to claim 8, it is clear that the memory controller (12/510) comprises logic capable of configuring the integrated circuit component (18/670) for operation with a companion integrated circuit component (20/672).

With regard to claim 9, it is clear that memory controller (12/510) comprises logic capable of configuring either the integrated circuit component (18/670) or (20/672) for operation in a stand-alone configuration.

With regard to claim 10, it is clear that the first portion of the system bus is substantially one-half of the system bus and the second portion of the system bus is a remainder of the system bus (see at least column 7, lines 4-9).

With regard to claim 11, Estakhri discloses a system comprising: a plurality of companion integrated circuit components (18/670, 20/672) that collectively implement a logic function embodied in a single, conventional integrated circuit component (shown generally at Fig. 1, 6(a, b), each companion integrated circuit component (one of 18/670, 20/672) comprising: a first logic interface for communicating with a remote component via a portion of a system bus (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 comprises the so-called "first logic interface" for communicating with a remote component via a portion of a system bus 28/260); a second logic interface for communication with companion logic interfaces of the remaining of the plurality of the integrated circuit components over a separate bus (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 comprises the so-called "second logic interface" capable of being configured to interface with a companion logic interfaces of the remaining of the plurality of integrated circuit (the other of 18/670 or 20/672) and to receive information that is communicated from the companion integrated circuit, which information was communicated to the companion integrated circuit via a second portion of the system bus (38/684); and logic (memory controller (12/510) for controlling the selective communication of information received

from the first logic interface (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 comprises the so-called "first logic interface" for communicating with a remote component via a portion of a system bus 28/260) via the portion of the system bus through the second logic interface to the companion integrated circuit (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 comprises the so-called "second logic interface" capable of being configured to interface with a companion logic interfaces of the remaining of the plurality of integrated circuit (the other of 18/670 or 20/672) and to receive information that is communicated from the companion integrated circuit, which information was communicated to the companion integrated circuit via a second portion of the system bus (38/684).

With regard to claim 12, as discussed in claim 11, the logic for controlling the selective communication of information received from the first logic interface through the second logic interface further includes first split bus logic configured to interface with the first logic interface, and second split bus logic configured to interface with the second logic interface (the system bus of Estakhri comprises a first split bus and a second split bus ;see at least column 7, lines 4-9).

With regard to claim 13, the link layer control logic in both first split bus logic and the second split bus logic (it is clear that the controller (12/510) provides unified bus logic configured to consolidate information received from both bus logics), the link layer control logic being configured to exchange link layer control information, such that both

the first split bus logic and the second split bus logic possess complete link layer control information for the data being communicated over the system bus (it is clear that the controller (12/510) provides unified bus logic configured to consolidate information received from both bus logics).

With regard to claims 15-19, see discussion above, since the subject matter presented in claims 15-19 has already been addressed above).

With regard to claim 20, Estakhri discloses an integrated circuit component comprising: a first set of conductive pins for channeling communications with a remote component via a portion of a system bus (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 comprises the so-called "first logic interface" for communicating with a remote component via a portion of a system bus 28/260; note also that it is inherent that pins must be provided for connections between discrete chips or ICs); a second set of conductive pins for channeling communications with a companion integrated circuit component (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 comprises the so-called "second logic interface" capable of being configured to interface with a companion logic interfaces of the remaining of the plurality of integrated circuit (the other of 18/670 or 20/672) and to receive information that is communicated from the companion integrated circuit, which information was communicated to the companion integrated circuit via a second portion of the system bus (38/684); note also that it is inherent that pins must be provided for connections

between discrete chips or ICs); additional conductive pins for carrying additional control and communication signals (it is clear that additional pins in addition to the conductive pins discussed above must be used in the IC of Estakhri); wherein the number of total conductive pins of the integrated circuit component is fewer than the number of conductive pins of a corresponding conventional integrated circuit component (as best the examiner can ascertain, the number of total conductive pins of the integrated circuit component of Estakhri is fewer than the number of conductive pins of a corresponding conventional integrated circuit component, since split bus system is used for each IC component).

With regard to claims 21-23, see discussion above, since the subject matter presented in claims 21-23 has already been addressed above.

With regard to claim 24, it is clear that "conductive pins" must also be provided so that different ICS (as identified above) can be connected to one another.

***Allowable Subject Matter***

Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 14 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

US Patent Nos. 5,862,359, 6,182,178, 6,871,257, 5,430,859, and PG Pub. No. 20050014397 are cited as relevant art.

Definition of Flash Memory from Wikipedia is also cited as relevant art.

Any inquiry concerning this communication should be directed to Khanh Dang at telephone number 571-272-3626.

Khanh Dang
Primary Examiner